A comparison between common-source and cascode topologies for V-band millimeter-wave MMIC Low Noise Amplifier design

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Abstract — In this paper, a three-stage cascode LNA and a three-stage common source LNA are presented. A comparison in terms of noise figure and gain between the two designed three-stage MMIC common source and cascode LNAs is discussed. This LNAs will be used as a part of a WPAN (Wireless Personal Area Network) receiver in the millimeter-wave band at 60 GHz.

These low noise amplifiers are designed according to the MMIC technology (Monolithic Microwave Integrated Circuit) in PH15 process from UMS foundry and uses a 0.15 μm GaAs PHEMT (Pseudomorphic High Electron Mobility Transistor).

The three-stage cascode LNA shows better performances compared to the three-stage common source LNA. The proposed three-stage cascode LNA exhibits a very low noise figure which is equal to 1dB and a high gain which is about 23 dB. An input return loss of -6.61 dB and an output return loss of -11.26 dB are also achieved by this LNA.

Keywords — Low Noise Amplifier, V-band, MMIC technology, LNA, amplifier, cascode, common-source, Pseudomorphic High Electron Mobility Transistor (PHEMT).

I. INTRODUCTION

The current challenge of wireless telecommunications is to ensure a higher transmission rates. For this, several solutions are being considered including the increase in frequency to millimeter wave spectrum.

Operating on the millimeter wave frequencies become attractive because of the availability of large free frequency bands. The band around 60 GHz is free to use and offers the possibility of data communication within short distance at speeds of several gigabits per second. This band is used for Wireless Personal Area Network (WPAN) which is governed by the standard IEEE 802.15.3c for multi-gigabit multimedia applications. [1]-[2]

These applications are possible due to the recent development in transistors performance. The progress in physics of semiconductors have been the origin of a new generation of components, called heterojunction transistors such as HEMT (High Electron Mobility Transistors). Another family of HEMTs, named "pseudomorphic" offers better noise performance. [3]-[4]

The high mobility of electrons in these transistors [4] allows operation at high frequencies (over 60 GHz). HEMT and PHEMT transistors, are used in particular for the low noise amplifier design working in the millimeter band, which is the subject of this work.

The LNA has a fundamental role in a RF receiver front end (Fig.1) [5]. Its main function is to provide a high gain to a signal, while adding a very low noise. It allows a level of exploitable signal with a minimum possible error.
Fig. 1 shows the architecture of the transmitter at 60 GHz. It consists of band-pass filters, a patch antenna network, a mixer, a frequency multiplier, a low noise amplifier and a power amplifier. The LO signal is provided by an external source that is not integrated in the module.

In this paper, we present the design of a low noise amplifier that will be used as a part of a WPAN receiver block working in the millimeter-wave band at 60 GHz.

Reported LNAs for 60 GHz applications achieve good gain values around 20 dB with a noise figure around 6 dB [6]-[7]-[8] or 2.5 dB [9]. These LNAs are composed of several stages.

The particularity of our LNA compared to other LNAs is its very low noise figure which is about 1 dB and its high gain that reaches 23.5 dB.

This circuit is designed using MMIC technology in PH15 process from UMS foundry. This technological process is based in PHEMT transistor with a length of 0.15 µm [12]. The studied model is characterized by a gate width of 30 µm and a number of fingers equal to 4.

II. LNA CIRCUIT DESIGN

A. Static study of PHEMT

a. Comparison between PH15 and PH25

In order to choose the adequate PHEMT transistor, we are going to do a performance comparison (minimum noise factor NFmin, and maximum gain MaxGain) between the two transistor PH15 and PH25 (PHEMT transistor with a length of 0.25 µm) by changing the number of fingers (N) and the gate width (W) of these transistors as shown in Tab.1. [13]

The MaxGain is the maximal gain possible if the input and the output are matched for maximum gain.

The NFmin is the minimum noise possible if the input and the output are matched for minimum noise.

Tab1. Performance comparison between different PHEMT transistors

<table>
<thead>
<tr>
<th>N/W (µm)</th>
<th>2/30</th>
<th>4/30</th>
<th>8/30</th>
<th>2/70</th>
<th>4/70</th>
<th>8/70</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>PH25</td>
<td>PH15</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MaxGain</td>
<td>8.369d</td>
<td>8.051d</td>
<td>6.016d</td>
<td>7.497d</td>
<td>6.852d</td>
<td>5.621d</td>
</tr>
<tr>
<td>NFmin</td>
<td>0.413d</td>
<td>0.413d</td>
<td>0.473d</td>
<td>0.472d</td>
<td>0.453d</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>NFmin</td>
<td>0.276d</td>
<td>0.250d</td>
<td>0.233d</td>
<td>0.476d</td>
<td>0.356d</td>
<td>0.326d</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

From the Tab.1 we can conclude that PH15 transistor gives better results (lower minimum noise figure and maximum gain) than PH25 transistor. We also see that the MaxGain increases by increasing the gate width (W) and NFmin decreases by reducing the number of fingers (N) of the transistor. Thus, the gate width and the number of fingers should be chosen carefully to have a compromise between a minimal noise factor and high Maxgain. Therefore, we choose to use a PH15 transistor with a gate width of 30 µm and a number of fingers equal to 4.

b. The bias point selection

The operating point must provide a compromise between a minimal noise factor (NFmin) and a high gain (MaxGain).

Fig. 2 and Fig. 3 respectively show the variations of NFmin and MaxGain according to Vds and Vgs. We choose the operation point (Vds = 2V, Vgs = 0V) represented by m1 and m2 in these figures. This point gives a better compromise between the gain and the noise figure.

![Fig. 2 NFmin as a function of Vds and Vgs](image2)

![Fig. 3 MaxGain as a function of Vds and Vgs](image3)

B. Dynamic study

After the static study of the PHEMT transistor, which led to the choice of the optimal bias point, we proceed to the dynamic study of the low noise amplifier.

We choose for this design a cascode configuration rather than a common source (CS) or common gate (CG)
configuration that are widely used for lower band frequencies. Compared to the CG or CS topologies, the cascade configuration shows better isolation and higher gain. It also has similar input linearity and input impedance matching as the CS topology [14]. Thus, we choose to employ a cascade topology for the 60 GHz LNA designed in this work.

a. Stability

When an amplifier is unstable, there is a risk of oscillations, due to reflection coefficients at the input and at the output of the transistor that are greater than unity.

Conditional stability (Stability Factor below 1) is when the stability of the quadruple is checked only for certain source impedance and load values at the operating frequency. If the stability conditions are satisfied whatever the impedance of the source and the load, the quadruple is then unconditionally stable (Stability Factor over 1).

Stability is important because it is affecting general LNA performance. Oscillations can be caused by several major causes such as: high gain, poor return loss and reverse isolation. For a low noise amplifier we must have an unconditional stability at the operating frequency. Fig.4 shows the stability factor of the designed V-band LNA.

From Fig.4 we can observe that the stability factor of the designed V-band LNA is more than 2 (Fig.6) for the full band from 0 GHz to 200 GHz. So, it is unconditionally stable around 60 GHz.

b. Impedance matching

Most of LNAs designed for such applications adopted distributed elements rather than lumped elements for impedance matching. In order to obtain good performance we made a compromise between the noise figure and the gain. The input matching is realized with a source impedance which favors a minimal noise figure. The output matching is realized with a load impedance to reach the maximal gain possible.

III. THREE-STAGE LNA COMMON-SOURCE STRUCTURE

Fig.5 shows an electrical schematic of the three-stage V-band LNA MMIC circuit in common-source configuration. The input and the output ports were designed to have a good matching with 50Ω load impedance to maintain sufficient load power in the high-frequency region around 60 GHz.

Fig.5 Electrical schematic of the designed three-stage common-source V-band LNA.

Fig.6 shows the Noise figure compared to NFmin. We observe that a good noise matching is obtained.

Fig.6 Noise figure.

Fig.7 shows the output gain of the proposed LNA compared to the MaxGain. We can see that the real gain perfectly matches the maximum.

Fig.7 Output Gain.
This LNA showed a low noise figure 1.625 dB (m4) and a high direct gain (S21) of 14.2 dB (m5) at 60 GHz.

Fig.8 shows the S-parameters simulation results of the proposed LNA.

![S-parameters simulation results](image)

Low reverse gain (S12) is desired to provide sufficient isolation and to simplify input and output matching. From Fig.8 we observe that S12 is lower than -30 dB. We can also see an input return loss (S11) of -25.88 dB and an output return loss (S22) of -26.79 dB at 60 GHz. S22 matching is observed near 60 GHz.

Fig.9 shows the compression point of the designed three-stage common-source LNA.

![Compression point](image)

We can observe in Fig.9 that the 1dB compression point of the proposed LNA is (Pin= -3.86 dBm, Pout=-34.13 dBm).

Fig.10 shows the third Intercept point (IP3).

From Fig.10 we observe that the designed LNA have a -4.452 dBm 3rd Order Output Intercept Point (OIP3).

IV. THREE-STAGE CASCODE LNA STRUCTURE

In order to improve the peak gain and obtain a lower noise figure at 60 GHz, we use a cascode configuration instead of a CS configuration. Fig.11 shows the electrical schematic of the three-stage LNA MMIC circuit in a cascode topology. The inter-stages matching was chosen to operate in the frequency band of 56 GHz to 62 GHz. [15]
Fig. 13 shows the output gain of the proposed LNA compared to the MaxGain. The gain of the three-stage cascode LNA was improved compared to the three-stage common-source configuration. In the previous configuration the gain was about 14.2 dB, now it reaches 23.5 dB.

From Fig. 14 we observe that the input return loss (S11) is about -6.61 dB and the output return loss (S22) reaches -11.26 dB. The reverse isolation (S12) is lower than -40 dB. A good matching is obtained near 60 GHz.

Tab. 2 shows a comparison of this work to some pervious low noise amplifiers in literature.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Number of stages</th>
<th>fopt (GHz)</th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>0.15µm PHEMT</td>
<td>3</td>
<td>66</td>
<td>6.21</td>
<td>17.3</td>
</tr>
<tr>
<td>[8]</td>
<td>65nm CMOS</td>
<td>2</td>
<td>58</td>
<td>5.3</td>
<td>17.5</td>
</tr>
<tr>
<td>[9]</td>
<td>100nm mHEMT</td>
<td>N/A</td>
<td>60</td>
<td>2.5</td>
<td>N/A</td>
</tr>
<tr>
<td>[10]</td>
<td>90-nm CMOS</td>
<td>4</td>
<td>60</td>
<td>3.7</td>
<td>15.3</td>
</tr>
<tr>
<td>[11]</td>
<td>0.15µm PHEMT</td>
<td>3</td>
<td>61</td>
<td>5.1</td>
<td>13.5</td>
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<td>13.5</td>
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</tbody>
</table>
As we can see this work demonstrate an LNA with a low Noise figure which is around 1dB and a high Gain that reaches 23.5dB which distinguish it from other LNAs in literature.

V. DISCUSSION

Tab.3 shows a comparison between the three-band cascode configuration and the three-stage common source configuration.

Tab.3 Comparison of common source and cascode configuration.

<table>
<thead>
<tr>
<th>configuration</th>
<th>Common source</th>
<th>Cascode</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>1.625 dB</td>
<td>1.029 dB</td>
</tr>
<tr>
<td>Gain</td>
<td>14.205 dB</td>
<td>23.506 dB</td>
</tr>
<tr>
<td>Reverse isolation</td>
<td>-30 dB</td>
<td>-40 dB</td>
</tr>
<tr>
<td>Compressing point</td>
<td>-34.131 dBm</td>
<td>7.337 dBm</td>
</tr>
<tr>
<td>Linearity (IIP3)</td>
<td>22 dBm</td>
<td>-3 dBm</td>
</tr>
</tbody>
</table>

From Tab.3 we can observe that the cascode configuration presents better results compared to the common source configuration. The noise figure is about 1 dB in the three-stage cascode LNA while it is equal to 1.625 dB for the common-source three-stage LNA. As for the gain, it reaches 23.506 dB for the cascode configuration which is higher than the gain obtained for the common-source configuration. The isolation for the three-stage cascode and the three-stage common-source are respectively equal to -40dB and -30dB. Hence, the common-source LNA presents a better linearity compared to the cascode LNA. The compression point for the common-source LNA and the cascode LNA is respectively -34.13dBm and 7.33dBm.

The three-stage cascode LNA demonstrates high power gain, good noise performance and high reverse isolation.

VI. CONCLUSION

In this work we describe the development of two low noise amplifiers designed to operate at the V-Band. The first LNA circuit uses a common-source configuration and the second one uses a cascode configuration. This LNAs uses the MMIC GaAs PHEMT transistor and operate at 60 GHz for WPAN applications.

As mentioned in section V of this paper, the best topology for a three-stage LNA is the cascode configuration. The reason is that cascode stage has good noise figure in mm-wave band. Moreover it has a higher gain and a better reverse isolation.

The designed cascode LNA shows excellent performances including input and output return loss of -6.61 dB and -11.26 dB respectively, a gain of 23.5 dB, and a noise figure of 1dB which distinguishes it from other LNAs in literature. The 3-dB bandwidth is from 56 Ghz to 62 Ghz.

REFERENCES

**BIOGRAPHY**

**Noha Al majid**, obtained a Master degree in Telecommunications and Micro-wave devices in 2013 at the National School of Applied Sciences of Fez. Currently preparing her PhD thesis in the Information Processing and Transmission Laboratory (LTTI) in Sidi Mohamed Ben Abdellah University (USMBA), Fez, Morocco.

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