

# Investigation In The Convergence Of The Evanescent Model And The Polynomial Model Including Effective Conducting Path Effect (ECPE): Applied To The Submicronic SG FD SOI MOSFET

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**Abstract:** we are presenting a convergence study of the evanescent model and the polynomial model with and without the Effective Conduction Path Effect. These analytic models of the electric potential in the channel are used to analyze the short channel effect for the submicronic SG FD SOI MOSFET. Hereby, we figure out the 2D Poisson equation and we analytically write the surface potential, the threshold voltage, the DIBL and the sub-threshold slope. The results show a good agreement of the evanescent model and the polynomial model including the Effective Conduction Path Effect with measures done by simulation tools.

**Keywords:** Evanescent and polynomial models, Effective Conduction Path Effect, surface potential, threshold voltage, DIBL, swing, SG FD SOI MOSFET.

## I. Introduction

Microelectronic researchers are in perpetual research for the speed and integration density of elementary components in regard to the ITRS [1]. The miniaturization of the components dimensions affecting the electric characteristics leads the conceptors to imagine other structures [2-7] rather than conventional MOSFET to conserve the long channel performances. The submicronic FD SOI MOSFET is one of these components that are attractive devices for low power high-speed VLSI applications because of their small parasitic capacitance [8].

Various models [9-15] have been developed to analyze the short channel effect (SCE) for the submicronic FD SOI MOSFET. Most of these models make use of the resolution of the 2D Poisson equation. The characteristic length  $\lambda$ , deduced from this resolution, is related to technological parameters of components [5 and 16] and relies on the adopted models and boundary conditions. Very few papers have dealt with the convergence of these models [17].

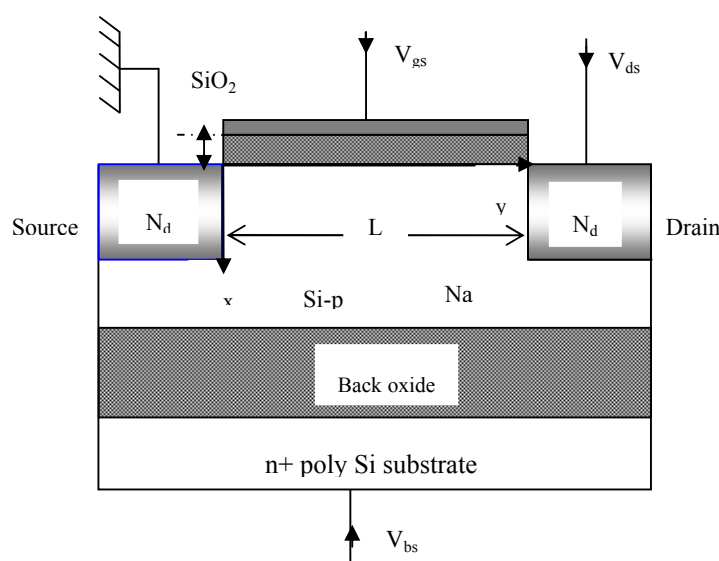
In this paper, we are interested in the convergence of the evanescent model and the polynomial models with and without the ECPE through the SCE for the submicronic Single Gate Fully Depleted SOI MOSFET. In the part II, we develop the evanescent model, with characteristic length  $\lambda_e$ , and draw the threshold voltage, DIBL and swing.

In the part III, we just recall the bases of the classical polynomial model as well as the characteristic length  $\lambda_p$ . Then, we take into consideration the ECPE and deduce the corrected characteristic length  $\lambda_{pc}$ . From one model to another, only  $\lambda_{i=e,p,pc}$  changes in the analytic expression of the surface potential, threshold voltage, DIBL and swing.

Simulators measurements are superposed for the validation of the obtained results.

## II. Evanescent Model

### II-1. Surface potential and threshold voltage.



**Figure 1:** Cross section of an n-channel SOI MOSFET

The structure SOI MOSFET (figure1) is completely depleted and the inversion charge is neglected in regard to that of the depletion. We define by  $L$  the channel length.  $t_{fox}$ ,  $t_{si}$  and  $t_{box}$  (or  $t_{fox/Si/box}$ ) represent respectively the thickness of the frontal oxide, the silicon body and the buried oxide.  $N_a$  is the silicon doping concentration under the frontal oxide and  $N_d$  is the doping concentration of the source and drain regions.  $\epsilon_{si}$  and  $\epsilon_{ox}$  represent respectively the dielectric permittivity of the silicon film and the silicon dioxide. The evanescent model supposes that the electrostatic potential in the silicon film is represented by  $\phi(x,y) = \phi_1(x) + \phi_2(x,y)$ .  $\phi_1(x)$  is the solution of Poisson equation for a long channel and  $\phi_2(x,y)$  is the solution of the Laplace equation and contain the short channel effect.

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_a}{\epsilon_{si}}. \quad (1)$$

The necessary boundary conditions of  $\phi_1$  and  $\phi_2$  to define  $\phi(x)$  are as follow:

For  $\phi_1$ :

$$\begin{cases} \phi_1(0) = V_{SL} = \frac{\bar{C}_{ox}}{C_{box}} \cdot \phi_{gf} + \frac{C_{box}}{C_{ox}} \cdot \phi_{gb} - \frac{qN_a t_{si}}{C_{ox}} \cdot (1 + \frac{C_{box}}{2C_{si}}) \\ \left( \frac{\partial \phi_1}{\partial x} \right)_{x=0} = \frac{C_{fox}}{\epsilon_{si}} \cdot (\phi_1(0) - \phi_{gf}) \\ \left( \frac{\partial \phi_1}{\partial x} \right)_{x=t_{si}} = \frac{C_{box}}{\epsilon_{si}} \cdot (\phi_1(t_{si}) - \phi_{gb}) \end{cases}$$

where  $\phi_{gf} = V_{gf} - V_{fbf}$  and  $\phi_{gb} = V_{gb} - V_{fbb}$ .

$V_{SL}$  represents the surface potential, at  $x = 0$ , for a long channel,  $V_{fbf}$  is the flat band voltage at  $x = 0$  and  $V_{fbb}$  is

the flat band voltage at  $x = t_{si}$ .  $C_{fox} = \frac{\epsilon_{ox}}{t_{fox}}$  is the

frontal oxide capacitance,  $C_{box} = \frac{\epsilon_{ox}}{t_{box}}$  is the buried

oxide capacitance and  $C_{si} = \frac{\epsilon_{si}}{t_{si}}$  is the silicon body

capacitance.  $\bar{C}_{ox}$ ,  $\bar{C}_{box}$  and  $C_{ox}$  represent the following expressions:

$$\frac{1}{\bar{C}_{ox}} = \frac{1}{C_{fox}} + \frac{1}{C_{box}} + \frac{1}{C_{si}}, \quad \frac{1}{\bar{C}_{box}} = \frac{1}{C_{box}} + \frac{1}{C_{si}} \quad \text{and} \quad C_{ox} = \frac{C_{fox} \cdot C_{box}}{\bar{C}_{ox}}.$$

For  $\phi_2$ :

$$\begin{cases} \phi_2(x, y = 0) = V_{bi} - \phi_1(x) \\ \phi_2(x, y = L) = V_{bi} + V_{ds} - \phi_1(x) \\ \left( \frac{\partial \phi_2}{\partial x} \right)_{x=0} = \frac{C_{fox}}{\epsilon_{si}} \cdot (\phi(x=0, y) - \phi_1(x=0)) \\ \left( \frac{\partial \phi_2}{\partial x} \right)_{x=t_{si}} = \frac{C_{box}}{\epsilon_{si}} \cdot (\phi(x=t_{si}, y) - \phi_1(x=t_{si})). \end{cases}$$

where  $V_{bi} = \left[ \frac{kT}{q} \cdot \ln \left( \frac{N_a N_d}{n_i^2} \right) \right]$  denotes the built-in

voltage between the source/drain end.

The frontal surface potential is defined as  $\phi_{sf}(y) = \phi_1(x=0) + \phi_2(x=0, y)$  and written as follow:

$$\begin{aligned} \phi_{sf}(y) &= V_{SL} + (V_{bi} + V_{ds} - V_{SL}) \cdot \frac{\sinh(y/\lambda_e)}{\sinh(L/\lambda_e)} \\ &+ (V_{bi} - V_{SL}) \cdot \frac{\sinh(L-y/\lambda_e)}{\sinh(L/\lambda_e)}. \end{aligned} \quad (2)$$

where  $\lambda_e$  represents the characteristic length for the evanescent model and verify the follow equality:

$$\frac{1}{\lambda_e} \cdot \sin\left(\frac{t_{si}}{\lambda_e}\right) - \frac{C_{fox}}{\epsilon_{si}} \left( \frac{C_{box}}{C_{si}} + \cos\left(\frac{t_{si}}{\lambda_e}\right) \right) - \frac{C_{box}}{\epsilon_{si}} = 0. \quad (3)$$

The threshold voltage is defined as a grid voltage

( $V_{gf} = V_{th}$ ) for  $\phi_{sf} = 2\phi_B$  where  $\phi_B = \left[ \frac{kT}{q} \cdot \ln \left( \frac{N_a}{n_i} \right) \right]$  is

the Fermi potential in the channel. This leads to write  $V_{th}$  as the form

$$\begin{aligned} V_{th} - V_{fbf} &= \frac{\bar{C}_{box}}{C_{ox}} \left\{ \frac{C_{box}}{C_{ox}} \cdot (V_{gb} - V_{fbf}) - \frac{qN_a t_{si}}{C_{ox}} \cdot (1 + \frac{C_{box}}{2C_{si}}) \right\} \\ &+ \left\{ \frac{2\phi_B \cdot \bar{C}_{box}}{C_{ox}} - (V_{bi} + V_{ds}) \cdot \frac{\sinh(y/\lambda_e)}{\sinh(L/\lambda_e)} - V_{bi} \cdot \frac{\sinh(L-y/\lambda_e)}{\sinh(L/\lambda_e)} \right\} \\ &\cdot \left[ \frac{1}{1 - \frac{\sinh(y/\lambda_e)}{\sinh(L/\lambda_e)} - \frac{\sinh(L-y/\lambda_e)}{\sinh(L/\lambda_e)}} \right] \end{aligned} \quad (4)$$

The gradient of threshold voltage is defined as  $\Delta V_{th} = V_{th0} - V_{th}$  where  $V_{th0}$  denotes the threshold voltage for a long channel FD SOI MOSFET [10] and written as:

$$\begin{aligned} V_{th0} - V_{fbf} &= \frac{\bar{C}_{box}}{C_{fox}} \cdot (V_{gb} - V_{fbb}) + 2\phi_B \cdot \frac{\bar{C}_{box}}{C_{ox}} + \frac{qN_a t_{si}}{C_{fox}} \cdot (1 - \frac{\bar{C}_{box}}{2C_{si}}). \end{aligned} \quad (5)$$

## II-2. Drain Induced Barrier Lowering

For the FD SOI MOSFET with short channel, the surface potential minimum increase with the drain

bias. Thus, the short channel effect is attributed to the penetration of the electric field line, of the drain-channel junction, in the channel resulting in the potential barrier lowering (DIBL effect). This leads to the decreasing of the threshold voltage.

The  $\mathfrak{R}$  parameter defined by  $\mathfrak{R} = \frac{\partial V_{th}}{\partial V_{ds}}$  evaluates the

DIBL effect and written as

$$\mathfrak{R} = \frac{\bar{C}_{box}}{\bar{C}_{ox}} \times \left\{ \frac{2 \sinh^2\left(\frac{L}{2\lambda_e}\right)}{K_1} \cdot \left(1 - \frac{K_2}{(K_2^2 - 4K_1K_3)^{1/2}}\right) - \frac{2V_{ds}}{(K_2^2 - 4K_1K_3)^{1/2}} \right\} \quad (6)$$

where

$$K_1 = \sinh^2(L/\lambda_e) - 4\sinh^2(L/2\lambda_e)$$

$$K_2 = (2\phi_B - V_{bi})\sinh^2(L/\lambda_e) - 2V_{ds}\sinh^2(L/2\lambda_e)$$

$$K_3 = (2\phi_B - V_{bi})^2 \sinh^2(L/\lambda_e) + V_{ds}^2$$

### II-3. Swing

The subthreshold slope, appealed swing, is defined as the grid voltage that modifies the drain current under a threshold of a decade and written as  $S = \frac{\partial V_{gs}}{\partial \ln(I_{ds})}$

where  $I_{ds}$  denotes the drain current.

Sean be written differently according to the minimum surface potential  $\varphi_{smin}$  :  $S = \ln(10) \cdot \frac{\partial V_{gs}}{\partial \varphi_{smin}} \cdot \frac{\partial \varphi_{smin}}{\partial \ln(I_{ds})}$ . As

the drain current is proportional to  $\exp\left(\frac{q\varphi_{smin}}{KT}\right)$ , this

leads to write S as the form

$$S = \frac{kT}{q} \cdot \ln(10) \cdot \frac{\partial V_{gs}}{\partial \varphi_{smin}} \quad (7)$$

The determination of the minimum surface potential  $y_0$  abscise allows to write the parameter S taking into consideration the short channel effect as

$$S = \frac{kT}{q} \cdot \ln(10) \cdot \frac{\bar{C}_{box}}{\bar{C}_{ox}} \cdot \left(1 - \frac{\sinh(y_0/\lambda_e)}{\sinh(L/\lambda_e)} - \frac{\sinh(L - y_0/\lambda_e)}{\sinh(L/\lambda_e)}\right)^{-1} \quad (8)$$

The corrective term

$$\gamma_s = \left(1 - \frac{\sinh(y_0/\lambda_e)}{\sinh(L/\lambda_e)} - \frac{\sinh((L - y_0)/\lambda_e)}{\sinh(L/\lambda_e)}\right) \quad (9)$$

denotes the short channel effect [13].

## III. Polynomial Model

### III-1. Without the ECPE

Considering the polynomial model [9] that considers the conduction current is at the surface of the silicon body and supposes parabolically the electrostatic potential profile in the vertical direction.

$$\phi(x, y) = C_0(y) + C_1(y)x + C_2(y)x^2 \quad (10)$$

Using the classical boundary conditions [4]

$$\begin{cases} -\phi(x=0, y) = \varphi_{sf}(y) \\ -\phi(x=t_{si}, y) = \varphi_{sb}(y) \\ -\frac{\partial \phi(x, y)}{\partial x} \Big|_{x=0} = \frac{C_{fox}}{\epsilon_{si}} \cdot (\varphi_{sf}(y) - \varphi_{gf}) \\ -\frac{\partial \phi(x, y)}{\partial x} \Big|_{x=t_{si}} = -\frac{C_{box}}{\epsilon_{si}} \cdot (\varphi_{sb}(y) - \varphi_{gb}) \end{cases}$$

and writing the Poisson equation as  $\varphi_{sf}(x=0, y)$ , we deduce the polynomial characteristic length

$$\lambda_p = (\epsilon_{si} \cdot t_{si} / C_{fox})^{1/2} \quad (11)$$

### III-2. Including the ECPE

The notion of the ECPE supposes that the gravity center of the conduction current is at  $x = d_{eff}$  [18]. The presentation of the electrostatic potential  $\phi(x, y)$  at  $x = d_{eff}$  allows us to bring about a correction to polynomial characteristic length  $\lambda_p$ .

The new corrected characteristic length corresponding to the polynomial model including ECPE is

$$\lambda_{pc} = \lambda_p \left(1 + \frac{C_{fox}}{\epsilon_{si}} \cdot d_{eff} - \frac{1}{2t_{si}} \cdot \frac{C_{fox}}{\epsilon_{si}} \cdot d_{eff}^2\right)^{1/2} \quad (12)$$

The evanescent model and the polynomial model with and without the ECPE are utilized to analysis the short channel effect. The analytic expressions of  $\varphi_{sf}$ ,  $V_{th}$ ,  $\Delta V_{th}$ ,  $\mathfrak{R}$  and S presented through the evanescent model remain adequate for the polynomial models with and without ECPE save for the characteristic length  $\lambda_{i=e,p,pc}$  which changes in the expressions.

## IV. Results and Discussion

In order to show the convergence situation of the already

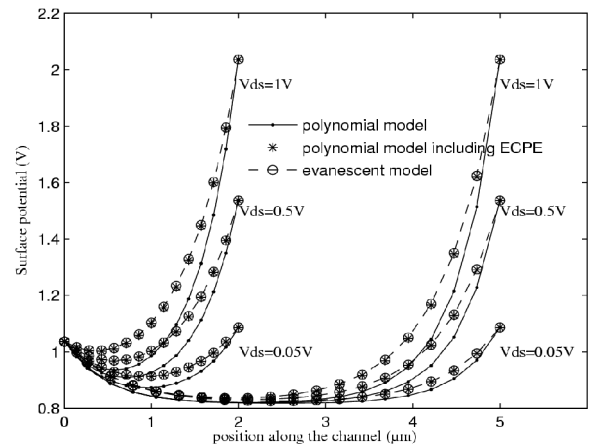
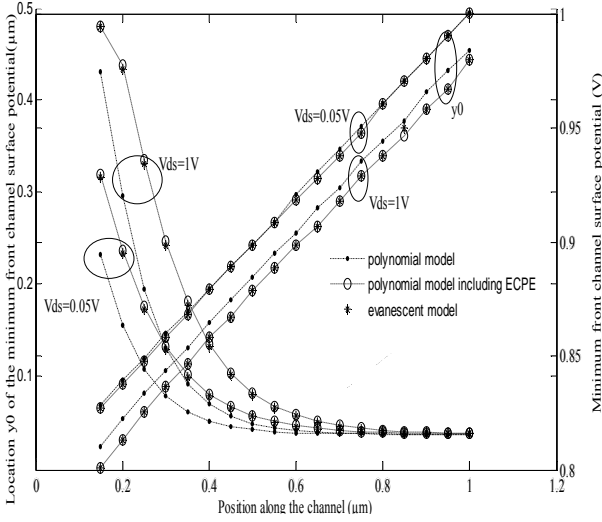


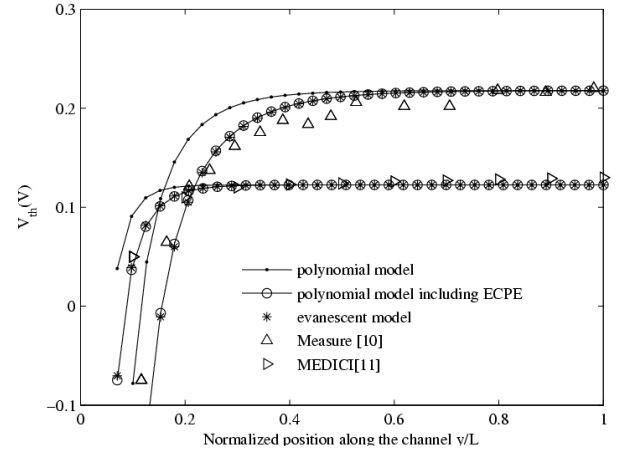
Figure 2. Surface potential versus position a channel length



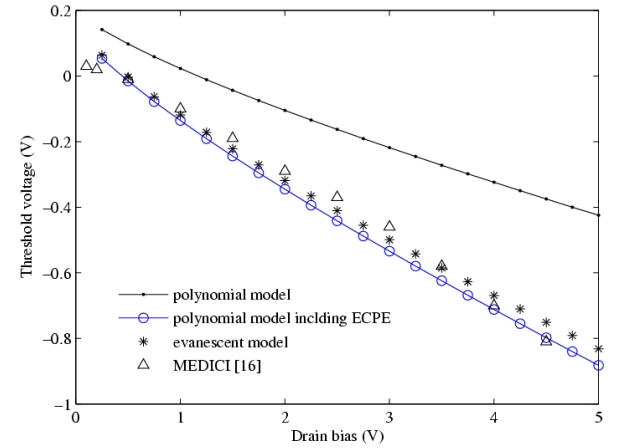
**Figure 3.** Minimum front channel surface potential and location  $y_0$  of the minimum front channel surface potential versus position along the channel for different values of  $V_{ds}$ .

mentioned models for the FD SOI MOSFET, we analyze the SCE via the surface potential, the threshold voltage, the DIBL and the swing. Measurements and/or simulator data are superposed the obtained results for validation. The same work for the conventional MOSFET prove that the convergence situation for the evanescent model and the polynomial model including ECPE is at  $d_{eff}=0.5t_{ox}$  [17].

For the three models, figure 2 shows the evolution of the surface potential along the channel for  $t_{fox/si/box}=9.2/80/300\text{nm}$ ,  $N_a=1.10^{17}\text{cm}^{-3}$ ,  $L=0.2$  and  $0.5\mu\text{m}$  and for  $V_{ds}=0.05, 0.5$  and  $1\text{V}$ . We notice an adequate convergence, at  $d_{eff}=0.35t_{si}$ , between the evanescent model and the polynomial model including the ECPE. We also see that the surface potential minimum increases, with the same drain bias, when  $L$  decreases. This leads to the decreasing of the channel barrier high. Figure 3 presents the evolution of the surface potential minimum and its position along the channel for  $t_{fox/si/box}=9.2/80/300\text{nm}$ ,  $N_a=1.10^{17}\text{cm}^{-3}$ ,  $L=0.2$  and  $0.5\mu\text{m}$  and for  $V_{ds}=0.05, 0.5$  and  $1\text{V}$ . The results, and on a large scale of drain bias, show a good agreement between the evanescent model and the polynomial model including the ECPE at  $d_{eff}=0.35t_{si}$ . Figure 4 illustrates the evolution of the threshold voltage in regard to the normalized position to  $L$  along the channel.



**Figure 4.** Threshold voltage versus normalized position along the channel  $y/L$



**Figure 5.** Variation of threshold voltage versus drain bias

These results prove a perfect agreement between the evanescent model and the polynomial model including the ECPE with Banna's measurements [10] as well as those of MEDICI's [13].

Figure 5 shows the evolution of the threshold voltage as function of drain bias for the submicronic FD SOI MOSFET with  $t_{fox/si/box}=10/50/200\text{nm}$ ,  $N_a=2.10^{17}\text{cm}^{-3}$  and  $L=0.140\mu\text{m}$ . The evolutions are almost linear as predicted by [20]. MEDICI's data [19] agree closely with the predictions of the evanescent model and the polynomial model including the ECPE at  $d_{eff}=0.35t_{si}$ . As the drain voltage increases, the channel barrier and the threshold voltage are reduced. This is called Drain Induced Barrier Lowering. Figure 6 illustrates the DIBL effect as function of the channel length for  $t_{fox/si/box}=1/10/50\text{nm}$ ,  $N_a=1.10^{17}\text{cm}^{-3}$  and  $V_{ds}=0.1$  and  $1.5\text{V}$ . The results, and on a large scale of drain bias, show a good agreement between the evanescent model and the polynomial model including the ECPE at  $d_{eff}=0.35t_{si}$ .

Figure 7 presents the swing parameter, in weak

inversion, as function of the channel length for  $t_{\text{fox/si/box}}=7/30/80\text{nm}$ ,  $N_a=3.10^{17}\text{cm}^{-3}$  and  $V_{\text{ds}}=0.1\text{V}$ . We notice an adequate convergence, at  $d_{\text{eff}}=0.35t_{\text{si}}$ , between the evanescent model and the polynomial model including the ECPE.

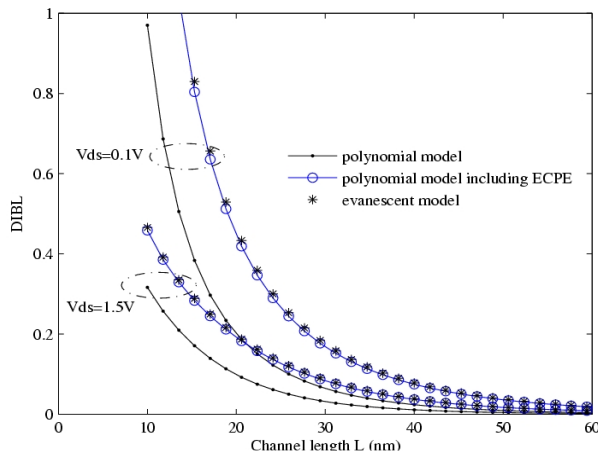


Figure 6. DIBL versus a channel length L

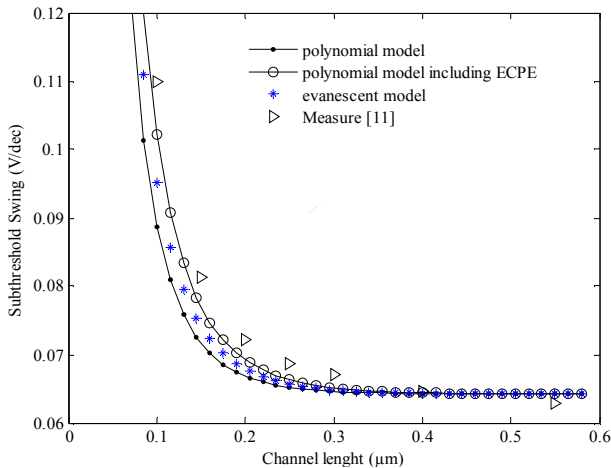


Figure 7. Subthreshold Swing versus a channel length

## V. Conclusion

The study of the short channel effects through the surface potential, the threshold voltage, the DIBL and the swing has proved the convergence of the evanescent model and the polynomial model including the ECPE. The convergence situation for the submicronic FD SOI MOSFET is at  $d_{\text{eff}}=0.35t_{\text{si}}$ .

## VI. References

[1] International Technology Roadmap for Semiconductors: 2001 Edition, 2002 Update. Available online at <http://public.itrs.net/>.  
 [2] A. Kranti, Rashmi, S. haldar, R. S. Gupta, "An accurate tow-dimentional CAD-Oriented model of retrograde doped MOSFETs for improved short channel performance," *Microelectronic Engineering*, vol 60, pp. 295-311, 2002.

[3] H. Kaur, S. Kabra, S. Haldar, R. S. Gupta, "An analytical threshold voltage model for graded channel asymmetric gate stack (GCASYMGAS) surrounding gate MOSFET," *Solid-State Electronics*, vol 52, pp. 305-311, 2008.  
 [4] A. Bouhdada and R. Marrakh, " Modeling of surface potential and threshold voltage of LDD nMOSFET's with localized defects," *Active and Passive Electr. Comp.*, vol 23, pp. 61-73, 2000.  
 [5] J. Lee, H. Shin, "Evanescent-mode analysis of short channel effects in MOSFETs," *Journal of the Korean Physical Society*, vol 44, n 1, pp. 50-55, 2004.  
 [6] A. Aouaj, A. Bouziane and A. Noua ry, " Analytical 2D modeling for potential distribution and threshold voltage of the short channel fully depleted cylindrical/surrounding gate MOSFET," vol 92, n 8, pp. 437-443, 2005.  
 [7] S. H. Oh, D. Monroe and J. M. Hergenrother, " Analytic description of channel effects in fully depleted double gate and cylindrical, surrounding gate MOSFET's", *IEEE electron device letters*, vol 21, n 9, pp. 445-447, 2000.  
 [8] J. P. Colinge, *Silicon-on-insulator technology: Materials to VLSI*. Amsterdam, The Netherlands: Kluwer, 1991.  
 [9] V. Aggarwal, M. Khanna, R. Sood, S. Haldar and R. S. Gupta, "Analytical tow-dimentional modeling for potential distribution and threshold voltage of the short channel fully depleted SOI ( Silicon On Insulator ) MOSFET ", *Solid-State Electronics*, vol 37, n 8, pp. 1537-1542, 1994.  
 [10] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen, M. Chan, "Threshold voltage model for deep-submicrometer fully depleted SOI MOSFET", *IEEE Transactions on Electron Devices*, vol 42, n 11, pp. 1949, 1995.  
 [11] A. Godoy, J. A. Lopez-Villanueva, J. A. jimenez-Tejada, A. Palma and F. Gamiz, " A simple subthreshold swing model for short channel MOSFET's ", *Solid-State Electronics*, vol 45, pp. 391-397, 2001.  
 [12] M. Chan, P. Su, H. Wan, C. H. Lin, S. K. H. Fung, A. M. Niknejad, C. Hu, p. K. Ko, " Modeling the floating bodt effects of fully depleted, partially depleted, and body grounded SOI MOSFET", *Solid-State Electronics*, vol 48, pp. 969-978, 2004 .  
 [13] A. Kumar, T. Nagumo, G. Tsutsui, T. Ohtou and T. Hiramoto, "Body factor conscious modeling of single gate fully depleted SOI MOSFET's for low power applications ", *Solid-State Electronics*, vol 49, pp. 997-1001, 2005.  
 [14] L. Ruizhen, H. Zhengsheng, "An analytic threshold voltage model for fully depleted SOI

MOSFETs”, Chinese Journal of Semiconductors, vol 26, n 12, pp. 2303, 2005.

[15] A. Ohata, M. Casse, O. Faynot, “Electrical characteristics related to silicon film thickness in advanced FD SOI-MOSFETs”, Solid-State Electronics, vol 52, pp. 126-133, 2008.

[16] D. Monroe, J. M. Hergenrother, “Evanescent mode analysis of short-channel effects in fully depleted SOI and related MOSFETs”, IEEE International SOI conference, Stuart, Florida, 1998.

[17] A. Bouziane, A. Aouaj, A. Nouaçry, «Comparison between the evanescent model, the polynomial model and the polynomial model including effective conduction path effect: applied to the submicronic

MOSFET », IEEE International Conf. on Multimedia Computing and System, Ouarzazate-Morocco, 02-04 April, 2009.

[18] T. K. Chiang, " A new scaling theory for fully depleted SOI double gate MOSFET's: including effective conducting path effect (ECPE)", Solid-State Electronics, vol 49, pp. 317-322, 2005.

[19] D. R. Poole and D. L. Kwong, " Tow-dimensional analysis modeling of threshold voltage of short channel MOSFET's ", vol EDL-5, pp. 443, 1984.

[20] Z. Kai, Z. Guohe, “A compact threshold voltage model for fully overlapped LDD FD SOI MOSFETs,” 2007, November, [Sciencepaper Online]. Available: <http://paper.edu.cn>.