Towards a new kind of component: Superconductor Single Electron Transistor SSET

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Single-electron transistors (SETs) are used to perform sensitive charge measurements and are widely discussed as possible components of dense integrated circuit. An exact model for a single-electron transistor (SET) was developed [1] early, within the circuit simulation package SPICE; it's constituted by two tunnel junctions, with two gates coupled to the island. We will present here a description of previews results of SET [1] and our perspective for a superconductor single electron transistor.
Superconducting single-electron transistors (SSET's) are small islands of superconducting material isolated from an external circuit by tunnel barriers (Josephson junctions). The normal tunnel barrier resistances: $R > R_Q = h / 4e^2 \approx 6.5$ KΩ are sufficient to constrain the excess charge on the island to integer multiples of e.
Key Words: Single electron transistor, SET, SSET, SNS-SET, junction, superconductor.

I. Motivation:

Microchips containing billions of transistors and operating with a clock cycle of billionth of a second are possible with the well controlled elaboration of materials such a pure Silicon single crystals.
The substantial potential of transistor for miniaturization, reliability and speed has been fully exploited.
According to the latest "roadmap" for microelectronics industry, and with the ongoing shrinking of transistors since 30 years as predicted by Moore law, the quantum aspect of electrons and atoms becomes very important in the manner how the devices will be building. What will be happens when the sizes of a transistor is comparable to a few atoms? Single electron transistors (SETs) are promising candidate for new nanoscaled devices.

III. The distribution probability of charge:

When a current is flowing through a single electron transistor, the charge on its island is not constant. In dynamic equilibrium, the probability $P(n)$ of a charge state n being occupied is constant and depends on the temperature and the voltages being applied. It is useful to know which of the charge states has the highest probability of being occupied. Here a formula for n_{opt} is derived that estimates the most probable charge state.
The relationship between the rates and the probabilities is:

II. Introduction:

The SET consists of two tunnel junctions (Fig. 1) connected in series and driven by voltage V; as a consequence, there exists a metallic island between the two junctions. This island is connected to a control voltage Vg via a capacitor Cg. These are called as gate voltage and the gate capacitance, respectively. The N describes the number of excess electrons in the island [1,3].

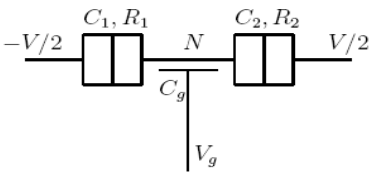

FIG. 1: Typical SET.

$$P(n) = P(n-1)\frac{\Gamma_{2L}(n-1) + \Gamma_{1R}(n-1)}{\Gamma_{2R(n)} + \Gamma_{1L(n)}}$$

The maximum of the probability distribution:

$$P(n^*\text{-}1) = P(n^*)$$

$$\Gamma_{2L}(n^*-1) + \Gamma_{1R}(n^*-1) = \Gamma_{2R}(n^*) + \Gamma_{1L}(n^*)$$

At low temperature:

For $\Delta E_i \langle 0 \rightarrow \Gamma_i \approx \frac{-\Delta E_i}{e^2 R_i}$

For $\Delta E_i \rangle 0 \rightarrow \Gamma_i \approx 0$

1) $V_1 > V_2$:

$$\frac{\Delta E_{1R}(n^* - 1)}{R_1} = \frac{\Delta E_{2R}(n^*)}{R_2}$$

This can be written as:

$$-R_2 V_1 + R_2 V(n^* - 1) + \frac{R_2 e}{2C_\Sigma} = R_1 V_2 - R_1 V(n^*) + \frac{R_1 e}{2C_\Sigma}$$ He

re, $V(n)$ is the voltage on the island for the nth charge state. Finally, solving for n^*,

$$n^* = \frac{-Q_0 - C_1 V_1 - C_2 V_2 - C_{g1} V_{g1} - C_{g2} V_{g2}}{e} + \frac{C_\Sigma (R_1 V_2 + R_2 V_1)}{e(R_1 + R_2)} + \frac{1}{2}$$

2) $V_1 < V_2$: Similar calculation yields the same result. The optimal charge state is halfway between n^* - 1 and n^*. The estimate for the most probable charge state is thus,

$$n^* = \frac{-Q_0 - C_1 V_1 - C_2 V_2 - C_{g1} V_{g1} - C_{g2} V_{g2}}{e} + \frac{C_\Sigma (R_1 V_2 + R_2 V_1)}{e(R_1 + R_2)}$$

IV. Inconvenient of SET:

The output impedance of SET operating at high temperature is typically much larger. This is a problem if the output of the SET has to drive a signal a long distance across the chip. The time it takes for the output of the SET to settle to the right value is RC where R is the output impedance of the SET and C is the capacitance of the wire that carries the signal away from the SET. Thus, the high output impedance can make the response of the circuit slow. Thus by adding the FET buffer stage at the output of the SET, the output impedance is reduced and will increase the speed of the circuit greatly.

V. Superconductor single electron transistor SNS-SET:

The model of SSET is illustrated by the schematic circuit diagram of the device (Fig. 2). Each SSET is bounded by two Josephson junctions, a gate capacitance, and a large mutual coupling capacitance Cm (Fig. 3).

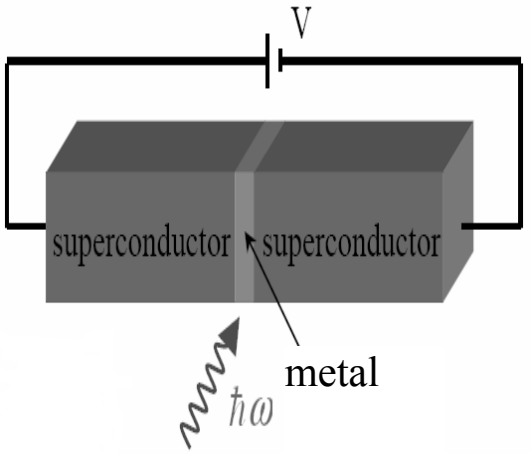

FIG. 2: Device of a SNS junction.

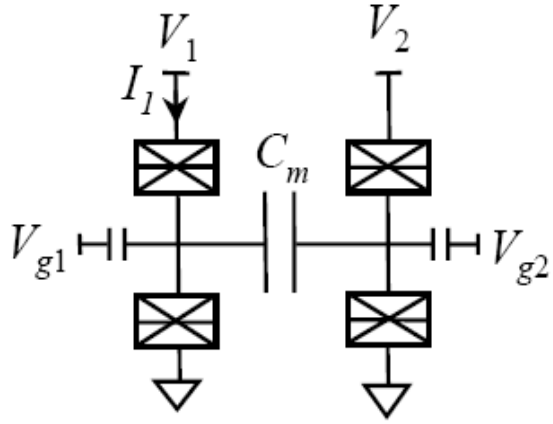

FIG. 3: Typical SNS-SET.

Experiments results show that in SNS, the tunnelling electrons to or from the island are done one by one and the transfer time is shorter [4,5]. In SNS-SET the proximity effect (P) plays an important role (penetration of the order parameter) SPS-SET [6].
If $\xi_N(T)$ (coherence length); $\xi_N(T) < L$
(width of the junction) which induce a gap energy Δ' into the central island so that: $\Delta' \sim E_T$ (Thouless energy)
$E_T = \hbar D/L^2$, as long as $E_T < \Delta$.
In addition to the Cooper pair current in the superconducting junctions, there also exists a current that consists of quasiparticles.
Moreover, the fluctuations in the electromagnetic environments cause also some structure to these currents.

VI. Synthesis;

A SNS-SET transistor can be used to measure charge either in the normal state or in the superconducting state. Typically, the SET

transistor is voltage biased at a point where there is a large modulation of the current as a function of the gate charge. The charge that is to be measured is coupled to the gate and the current through the gate is monitored. By this means; charges much smaller than the charge of an electron can be measured. SET transistors offer by far the best charge resolution of any of the available charge measurement devices. The charge resolution of the SNS-SET transistor will be better in the superconducting state due to the larger current modulation at the optimum bias point and the tunnelling time will be shorter in SNS-SET. We will use the Bose-Einstein distribution instead of Fermi-Dirac one. Our perspectives are to modelling and simulate a SSET for a programmable SET logic which will provide the potential for low power, intelligent LSI chips suitable for mobile applications.

REFERENCES:

[1] Günther Lientschnig, Irek WeymannL, and Peter Hadley, Jpn. J. Appl. Phys. Vol. 42 (2003) 6467

[2] K.K.Likharev et al Proc IEEE, 87 (1991) 606

[3] K.KLikharev et al, Proc of Int Semi-Cond Device Res.Symp, University of Virginia Charlottes ville, VA, (1995) 355.

[4] M.Devoret et al, Image de la Physique, (1991) 85.

[5] L.Geerligs et al, Phys Rev Lett., 64 (1990) 2691

[6] A. J. Manninen, R. S. Poikolainen, T. V. Ryynaänen, and J. P. Pekola Phys..Rev., B59 (1999) R14161