

# Class D Audio Amplifier with Trim-able Ramp Generator Design Theory and Design implementation for portable applications

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This paper presents a single chip class D amplifier with two selectable gains 6dB & 9dB, 1.4 W output power and 86% efficiency with an 8 ohm load. This chip uses a frequencies trim-able ramp generator. Input Clock Frequency Range with 250kHz – 550kHz and 8 bits trim, 4 bits (LSB) to trim the ramp amplitude to  $v_{dd}/5$  peak-to-peak, 4 bits (MSB) to adjust the ramp continuity, the trimming procedures consists on putting a zero input signal, and adjust the trim code such as to get a 50% duty cycle Pulse Wide Modulation output signal, Reduction of inter-modulation in case of mixing of Audio and Voice.

It operates with a 2.5 V to 5.5V supply voltage, 0.5  $\mu$ m, double-poly, triple-metal BiCMOS process. It has an area of 1.5 x 1.2 mm<sup>2</sup> and it achieves a THD as low as 0.04%, with a flat band response between 20 Hz and 20 kHz.

**Keywords** – single chip class D, selectable gains, trim-able ramp, output power, efficiency.

## I. INTRODUCTION

Traditionally class AB audio amplifiers have been used for driving a speaker load in portable devices including cell phones. However, their power efficiency is typically less than 20%, which reduces the overall systems battery lifetime and increases the heat dissipation. Class-D audio amplifiers achieve higher power efficiency by using pulse-width modulation (PWM), however a class D amplifier with conventional PWM modulation requires a bulky output filters [1 - 4]. High-end class-D amplifiers relax the output filter requirements by using extended digital signal processing to accomplish a modulation scheme that lies in between natural and uniform PWM.

This paper presents a class D amplifier for portable devices with trim able synchronous ramp generator to reduction of inter-modulation in case of mixing of Audio and Voice and eliminates the requirement of an output filter by using a double-sided natural sampling PWM [5].

Furthermore higher integration is achieved by using a fully differential architecture, which removes the need for input capacitors.

The proposed scheme was experimentally verified with a Synchronous Mode with 3 supported frequencies 294, 320 and 333, 3 kHz ramp generator prototype embedded in a class-D amplifier built in a 0.5- $\mu$ m CMOS process, which achieved 28mV amplitude accuracy with current consumption of 20  $\mu$ A.

The ramp is generated by constant charging current into the capacitors C1 and C2, which is connected between the ground and successively current source and current sink. The value of two capacitors is  $C1=C2=25$ pF.

The amplifier achieves a power efficiency of 86% delivering up to 1.4W output power to an 8 ohm load, and operates with a 2.5V-5.5V supply.

The design has been implemented in a 0.5  $\mu$ m, double-poly, triple-metal, BiCMOS process and occupies 1.5mm x 1.2mm. This amplifier achieves higher level of on-chip

integration and power over than previously reported class-D audio amplifiers [1 - 4].

## II. DESIGN THEORY

Currently most class D amplifiers use a binary PWM scheme in a H-bridge output configuration, which devices, or a half bridge architecture that requires high supply voltages and an output inductor [2 - 4].

Considering a pure resistive load switching the full bridge or the half bridge output of previously reported designs [2 - 4], the power supply voltage would be across the load resistance (plus resistance of the switches) with no input signal. The resulting current would be a square wave with magnitude equal to the power supply divided by the resistance of the load. For example, a full bridge using a 5V supply driving an 8 ohm load would conduct a current approximately equal to 0.5 A, and this is with no signal [5, 6]. Most designs currently solve the problem by providing some current limiting device in series with the speaker, usually a post-filter comprised of inductors and capacitors [2 -4]. Another solution widely used on high end class D amplifiers requires extended signal processing capabilities in order to accomplish a modulation scheme that lies in between natural and uniform PWM and thus generates the least amount of harmonics in the audio band.

### A. PWM (Pulse Width Modulation)

Several modulation techniques exist. The simplest is Pulse Width Modulation, where at a fixed frequency, the audio amplitude is compared to a triangle shaped wave and the duty cycle of this comparison contains the original amplitude (Fig. 1).

The differential pre-filtered output varies between positive and negative VDD, where filtered 50% duty cycle yields 0V across the load.

Since the "Average" signal can have up to 20 kHz frequency content, the amplifier runs on high frequency.

250 kHz are a common trade-off between accuracy and efficiency. A lower switching frequency offers higher amplifier efficiency and better THD but requires larger external filter. A higher switching frequency reduces the size and cost of the filter components at the expense of THD and efficiency [4].

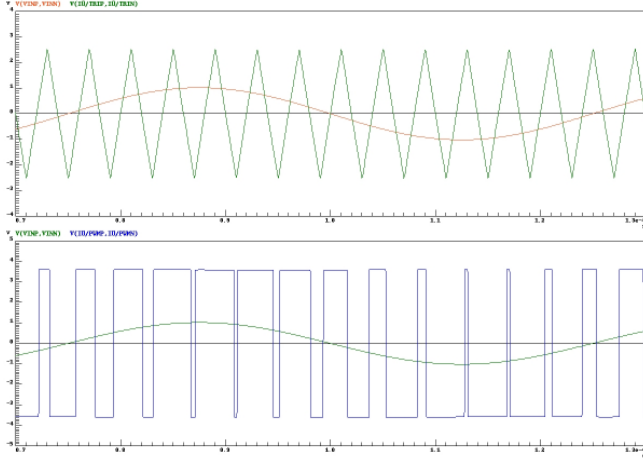


Figure 1– PWM signal

### B. Stability

This system has stability threshold limiting the systems bandwidth [6]. This limit may be calculated, considering the slope of the ripple signal ( $V_r = V_{\text{ripple}}$  on Fig 4) lower than the slope of the triangle wave ( $V_{tr}$ ) as shown Fig. 5. This consideration has been done for correct functioning of the system

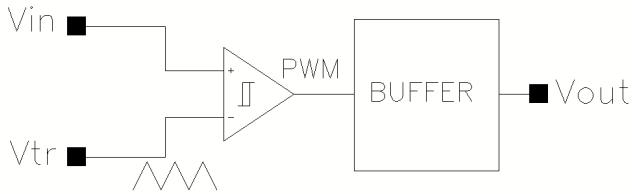


Figure 2 – Class-D basic schematic

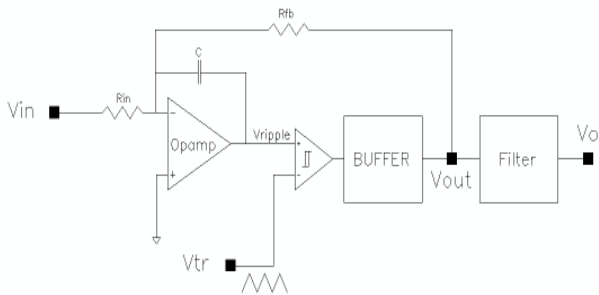


Figure 3 – Class-D schematic with feedback loop

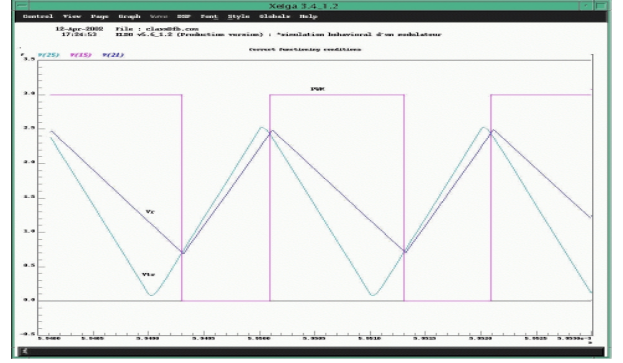


Figure 4 – Correct operating condition

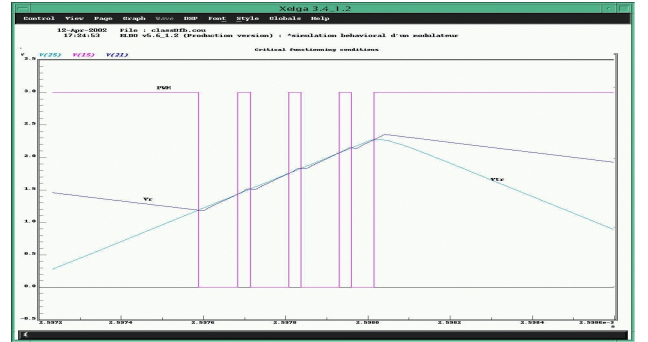


Figure 5 – Critical operating condition

If this condition is not met, the system may produce repeated output switching at intervals equal to the delay of the chain delay, defined by the PWM stage and by the output buffer stage, as shown on Fig. 5.

By converting this concept into formulas:

$$Ptr = 4.Vtr.fsw \quad (\text{Slope of triangle waveform}) \quad (\text{Eq. 5})$$

$$Pvr = \frac{1}{C} \left( \pm \frac{Vcc}{Rfb} - \frac{Vin}{Rin} \right) (\text{Slope of the ripple}) \quad (\text{Eq. 6})$$

Therefore, the boundary condition is

$$\frac{1}{C} \left( \pm \frac{Vcc}{Rfb} - \frac{Vin}{Rin} \right) \leq 4.Vtr.fsw \quad (\text{Eq. 7})$$

## III. DESIGN IMPLIMENTATION

### A. Top view

The top schematic view of Class-D amplifier (Fig. 6) is composed by a main part (inverting input integrator, triangle generator, PWM modulator, gate driver and MOSFET H-bridge) and secondary parts like common mode voltage and bias current generator, startup and protection circuit, input gain selector and shifter. All these parts are described in this chapter.

Two analogous power supplies (tailed together with decoupling capacitor on the circuit board) are used [1],

PVDD/PGND supply the MOSFET H-bridge where as AVDD/AGND supply the rest of circuit. A digital VDD is used to supply level shifter. ESD protection and bonding are not shown in this schematic but have been taken into account for simulation.

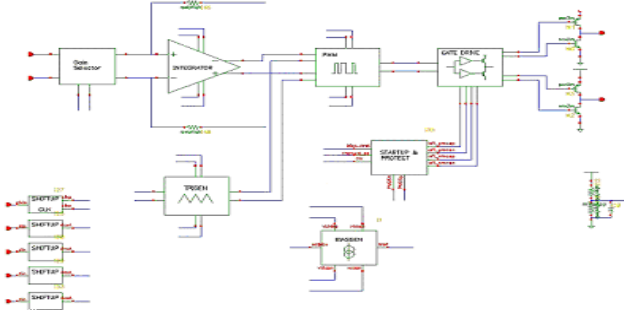


Figure 6 – Class-D Schematic.

### B. The proposed Triangle Generator

The proposed ramp is generated by constant charging current into the capacitors C1 and C2, which is connected between the ground and successively current source and current sink. The value of two capacitors is  $C1=C2=C=25\text{pF}$ .

The current through R1 is the charging current, kept constant by forcing the voltage across R1 to equal  $V_{DD}/2$  by op amp, configured as follower voltage.

The ramp slope is:

$$\frac{dV_{\text{ramp}}}{dt} = \pm \frac{V_{dd}}{2R1 * C} \quad (\text{Eq. 8})$$

The resistance R1 is adjusted by four digital bits Trim<3:0> for adjust finally the current charging, the ramp slope and V<sub>ramp</sub> peak-to-peak to equal  $V_{dd}/5$ .

The charge make in two phase  $\Phi1$  and  $\Phi2$ :

- In the phase  $\Phi1$ , the switches  $\Phi2$  will be open and the switches  $\Phi1$  will be closed, the capacitor C1 will be in charge by constant current and the ramp output is the charge voltage of C1, thus V<sub>out</sub> will be :

$$V_{out}(t) = \frac{V_{dd}}{2R1 * C} t + (V_{dd}/2 - R2 * I) \quad (\text{Eq. 9})$$

At the same time the capacitor C2 is in pre-charge state.

$$V_{C2}(t) = (V_{dd}/2 + R2I) (1 - \exp(-t/R2C))$$

- In the phase  $\Phi2$ , the switches  $\Phi1$  will be open and the switches  $\Phi2$  will be closed, the capacitor C2 will be in discharge by constant current, thus V<sub>out</sub> will be :

$$V_{out}(t) = -\frac{V_{dd}}{2R1 * C} t + (V_{dd}/2 + R2 * I) \quad (\text{Eq. 10})$$

In the same way the capacitor C1 is in RC discharge.

$$V_{C1}(t) = (V_{dd}/2 + R2I) (2 * \exp(-t/R2C) - 1)$$

The resistor R2 is adjusted by four digital bits Trim<7:4> to adjust the value of outp and outn, such that  $\Delta V=0$  (Fig.7).

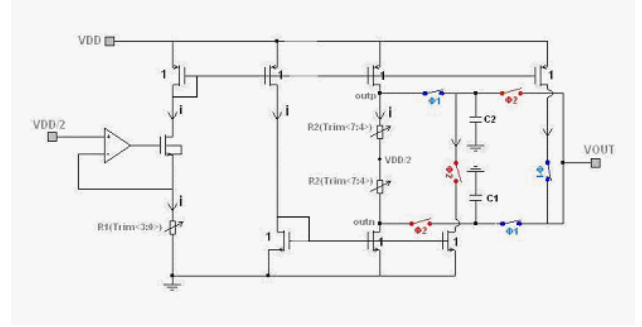


Figure 7 – proposed triangle Generator Schematic.

The condition to get the continuity of the ramp output is Trim<7:4>=0001, i.e. the value of  $R2=23.4\text{Kohms}$ .

The condition to get ramp slope or ramp output peak-to-peak equal  $V_{DD}/5$  is Trim<3:0>=0101, i.e. the value of  $R1=105\text{Kohms}$ .

The third condition is that the half period  $T/2$  will be large enough such that C2 voltage achieves 95% of its final value (i.e.  $V_{dd}/2 + R2I$ ), thus:

$$\exp\left(\frac{-T}{2R2C}\right) = 0.05 \quad (\text{Eq. 11})$$

So the minimum input clock period is  $T_{\min}=2 * R2C * \ln 20 = 3 * R2C = 1.725\mu\text{s}$

So the maximum input clock frequency  $F_{\max} = 580\text{ kHz}$

At top class D level, we can adjust the value of two resistors R1 and R2, by putting on both inputs (positive and negative) of the class-D a constant signal equal to  $V_{DD}/2$  (i.e. a zero differential input signal is going to the class-D).

Then we adjust the value of Trim such as to have on both outputs of the class-D a square signal with duty cycle equal 50%.

### IV. ARCHITECTURE AND CIRCUIT DESIGN

In order to implement the new scheme, a single monoaural channel has as much complexity as a stereo version of the traditional modulation scheme. As such, the issues of crosstalk are exacerbated, with twice as many independent switching edges to cause crosstalk problems.

Although layout techniques assist in isolating switching noise from coupling into sensitive nodes, circuit techniques such as chopping compensation and PWM deglitch logic, are also used to maximize performance.

When regulating current through an inductive load using switching methods, voltage spikes are induced onto the power and ground of the H-bridge. These spikes are due to the switching of current through the inductance of the bond wires and package pins, and are made worse with reverse-recovery currents in the back-body diodes of the power FETs. The voltage and current spikes can be coupled onto the power and ground signals of the analogous and PWM circuits. Layout techniques such as guard rings and careful power and ground routing can minimize the spikes induced onto the sensitive linear sections. For a fully integrated solution, the previously mentioned

switching noise on the IC is a concern, and it is quite likely that the switching noise from one of the half-

circuits will have an influence on the other half, which is much like crosstalk. In this example, the falling edge transition of OUTN occurs earlier than OUTP (Fig. 8).

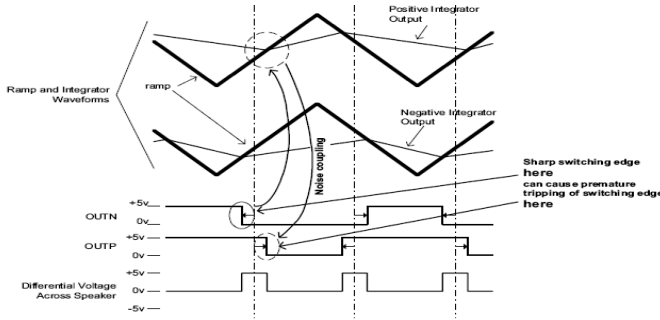


Fig. 8 Illustration of Cross-Coupling within a Monoaural Channel where using the Quaternary Modulation Scheme

The concern is that the switching of the negative half- circuit will couple disturbances onto the output of the positive half-circuit's integrator, making OUTP trip prior to its expected crossing point. This problem would manifest itself near zero crossing where audio signals are smallest and most likely to exist. To eliminate the potential of "crosstalk" within one channel, a time delay is introduced into the system.

This has the main effect of moving the susceptible crosstalk point away from zero crossing to a higher power level. For low-end audio applications, such as cell phones and mp3 players, this is not noticeable.

Fig. 9 shows the schematic of the class D amplifier with the new modulation method.

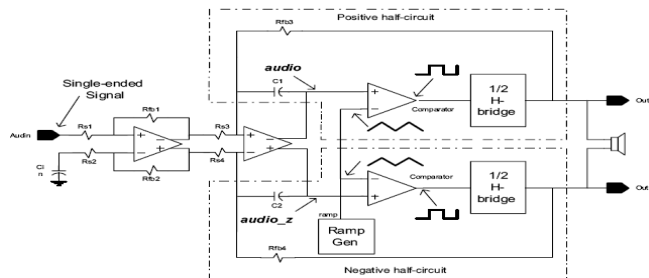


Fig. 9 Schematic of the Designed Class -D Audio Power Amplifier.

The circuit is divided into positive and negative half-circuits. These two half-circuits operate in inverse phase to each other, which requires a fully differential pre amplifier to create both an audio signal (audio) and its inverse (audio\_z). The fully-differential analog stage allows the inputs to be biased at a voltage other than mid-supply. It also eliminates the requirement for a bypass capacitor and input decoupling capacitors. It improves the RF immunity of the amplifier as well. The amplifier utilizes two feedback loops. The first one pre-shapes the audio signal before it is compared to a triangular waveform to form the PWM signal. The second loop sets the gain for the amplifier.

The output stage consists of two high gain comparators, deglitch logic and output FETs. On the positive side of the circuit, the audio frequency analog signal (audio) is compared with a signal from the ramp generator, and the resulting pulse-

width modulated signal is supplied to the half-full-bridge. Similarly, the negative side of the circuit uses the same ramp signal, but uses an inverse analogous signal (audio\_z). However, note that the comparator and full bridge positive and negative outputs switch at the same time when the differential input signal is zero. The resulting differential waveform across the load becomes zero.

When a positive audio signal is present, waveforms change to that shown in Fig. 2, the edges of OUTP move away from each other, and the edges of OUTN move towards each other. The resulting differential signal across the bridge tied load consists of narrow pulses with polarity determined by the polarity of the audio input signal. These narrow pulses also have a secondary desired effect of doubling the differential PWM frequency. This effect also achieves the desired effect of placing current into the load only when needed, resulting in increased efficiency and less energy loss in the speaker. The modulation phase that regulates the current through the load by applying the power supply voltage at reverse polarity is eliminated; hence the output of the full bridge can be placed directly across the load.

## V. EXPERIMENTAL RESULTS

The class D audio amplifier has been integrated in a 0.5um, double-poly, triple-metal, BiCMOS process, occupying an area of 1.5 x 1.2 mm<sup>2</sup>. The measured output peak current was measured to be 0.35A into an 8 ohm load, using a 3.6V supply voltage. The IC consumed 2.5mA of quiescent current under those conditions with an rms output power of 0.5W and a power efficiency of 79%. A power efficiency of 86% was achieved at a supply voltage of 6.5V. Fig. 10 shows the efficiency versus power curve. The total harmonic distortion plus noise (THD+N) was measured with an Audio Precision (AP) measurement system. A lowpass filter had to be used at the output since the AP measurement system can not handle pure class D audio amplifiers because of the high frequency PWM waveform. The THD+N measured under the above-mentioned conditions varies from under 0.04% at low frequencies to a maximum of 0.4% at 7 kHz. Fig. 11 shows a plot of the THD+N versus the power under different supply voltage levels. Fig 12 shows layout of Amplifier Class D with process 0.5 um. Table 1 summarizes the measured results. The output offset is higher than predicted in the simulations because of mismatch in the feedback and in the input resistors.

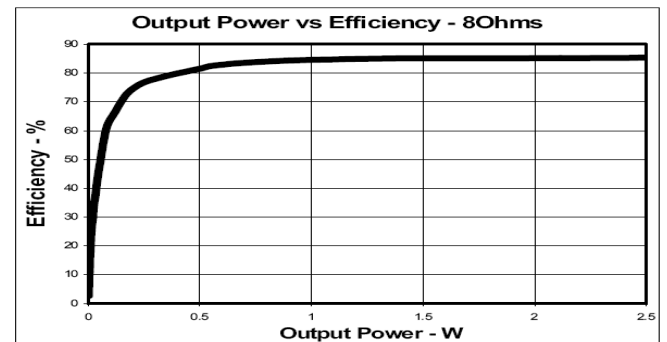


Fig.10. Efficiency versus Power Curve

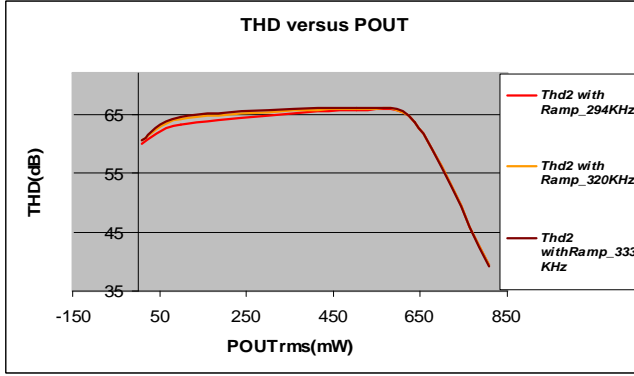


Fig. 11 shows the THD+N versus the power.

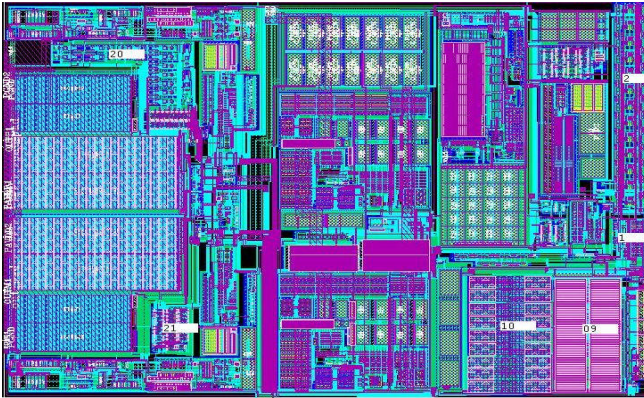


Fig. 12. Layout of Amplifier Class D with process 0.5um of Texas Instrument.

## VI. CONCLUSIONS

We have presented a new class D audio amplifier for low voltage applications with high efficiency and minimum system solution size. The amplifier is a great improvement over its class AB counterparts where it comes to battery powered application since it dissipates less power in the amplifier itself.

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Output Power	1.4	V
Speaker Load	4 or 8	ohm
Total Harmonic Distortion Plus Noise <i>THD+N</i>	0.11	%
Common Mode Rejection Ratio CMRR	69	dB
Power Supply Rejection PSRR	75	dB

TABLE I: SUMMARY OF MEASUREMENT RESULTS

1. Level Shifters (35 Cells) (DVDD to VBAT)
2. Level Shifters (05 Cells) (AVDD to VBAT)
3. Main Bias Generator
4. Synchronous Ramp Generator
5. Vmid Generation for Ramp Generator and Analog
6. Digital Start-Up State Machine
7. Amplifiers (2 Cells: Pre-Amplifier, Integrator)
8. Integration Capacitors, Switchs and Filters
9. Local Bias Generator
10. Clamping Circuit (Option disabled by default)
11. Fast Comparators (2 Cells)
12. Level Shifter for Driver (2 Cells)
13. Pulse Generator for Deglitch
14. Gate Driver (2 Cells)
15. H-Bridge Power MOS (2 Nmos, 2 Pmos)
16. Analog Test
17. Digital Test
18. Digital Control of Ramp Clocks
19. Routing

Parameters	measurements	unity
Supply Voltage	3.6 -5.5	V