GROWTH OF SILICON BY LIQUID PHASE EPITAXY AT LOW TEMPERATURE: APPLICATION TO THIN FILM SOLAR CELLS

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Growth of silicon thin layer by Liquid Phase Epitaxy (LPE) at low temperature (800 °C) can be an attractive technique to fabricate low cost photovoltaic cells. Using a two baths technique, one can remove native oxide and then obtain homogeneous layers presenting a p/p+ structure. Short circuit current of 19 mA/cm² and conversion efficiency of 4.7% are obtained with 12 µm thick layer.

Keywords: LPE, silicon, thin film, solar cells.

I–Introduction

The reduction of silicon substrate thick is a major axis to decrease the cost of solar cells fabrication and marketing. The growth of thin films of silicon by liquid phase epitaxy (LPE) at low temperature (down to 800 °C) is very promising to realize a n+/p structure at weak thickness (< 50 µm). With 50 µm solar cells it's possible to obtain efficiency near a classical solar cell because this thickness is sufficient to absorb 80 % of incident photons of the solar spectra.

This technique is compatible with development lasting because it ensures an economical energy (procedure at low temperature, absence of liquids and gaseous discharges). In our case this simple technique can be used to obtain silicon single crystalline thin films transferable on foreign substrates at low cost like ceramic or glass [1]. Liquid phase epitaxy at high temperature (> 950 °C) has been widely studied in classical solvents like tin and indium [2]. At low temperature, the growth of thin films from melt Al-Ga [3] and Au–Bi [4] has been demonstrated. But, in the case of Al-Ga alloy, the layers obtained were highly doped and not used for solar cells fabrication. So, to obtain films weakly doped, we have studied some solvents like In, Sn, Pb and their alloys at the low temperature (700–800 °C) [5]. Among all these solvents, tin gives good results (smooth and homogeneous layers).

II–Realization of epitaxial layers

In this study, the epitaxial growth is carried out in a graphite crucible of sliding boat type mounted in horizontal quartz tube. The growth of layers is realized on of CZ single crystalline Silicon substrate, (111) orientation and (≤ 0, 01 Ω.cm resistivity).

To obtain Silicon single crystalline weakly doped (< 10^{17}at.cm^{-3}), we have implemented, an epitaxial growth technique at two melts, the first one (Al–Sn) is used to reduce native silicon oxide on surface silicon on which we wish to do the epitaxial growth. And the second one (Sn–Ga) serves to grow silicon active layers weakly doped by Ga [6].

After saturation of melts by silicon at 800 °C, the substrate is put in contact with Sn–Al melt a few minutes. Al reacts with SiO_2 and forms Al_2O_3 compound which migrates of melt-substrate interface until melt surface. Then, the substrate is placed under Sn–Ga melt. The system is cooled down at a rate of 0.5 °C/min under argon or hydrogen flow. The separation between cleaning step and growth step avoid the pollution problem of growth melt by Al.

The strategy to reach two objectives: cleaning melt without hydrogen and LPE at low temperature, consists to study finely the composition of melts by thermodynamics considerations for ternary or quaternary alloys.

Smooth and homogeneous silicon Layers of 10 to 17 µm thick (after 2 at 3h of growth) have been obtained according this technique (figure1).

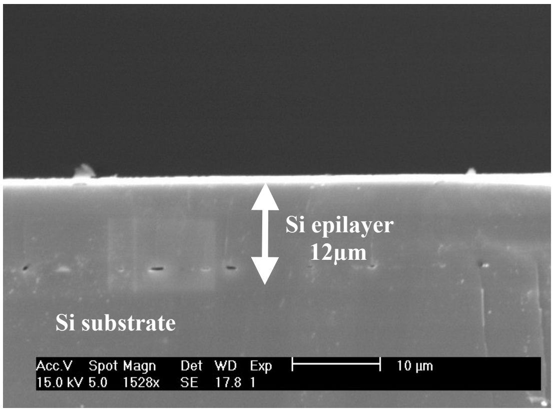
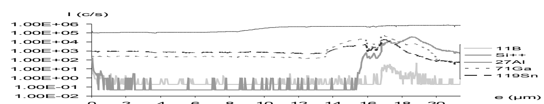


Fig. 1 : SEM micrograph of Si layer grown at 800°from pure Sn

According to SIMS analysis (figure2) performed on epitaxial layers obtained at 800 °C during 3 hours of growth, we have remarked an aluminum diffusion at interface «epitaxial layer/ silicone substrate », which gives Silicon structure of p (active layer) / p^+ (aluminum–silicon) type.



Incorporation of Ga is enough homogeneous in the active layer and Al still confined in the intermediate layer. These analyses show also that interfacial layer p^+ (Al) is in the 2 – 3 µm range and that active layer is in the 10 – 13 µm range. It's necessary to note that this layer highly doped p+ can be used effectively like BSF (Back Surface Field).

III–Realization of solar cells

Among these layers, several solar cells have been established resulting by phosphorus diffusion (20 min at 850°C) to form n^+/p junction of 0.3µm thick. Metallic contacts on the front side have been realized by evaporation under vacuum thanks at deposition of 3 layers Ti–Pd (100 nm)–Ag (1 – 1.5 µm); on the rear side, has been deposed, by the same technique, an Aluminum layer (1 – 1.5 µm). Finally, a SiN_x: H antireflective coating (70nm thick) has been deposed by PECVD on the front side of solar cell which gives a secondary affect of passivation of electronic defects by hydrogen [7]. After these steps of elaboration, solar cells have been tested electrically and AM1.5 spectra.

The first results obtained before and after the antireflective coating show that photogenerated current density (Icc) is in 8–10 mA/cm^2 range before deposition, it increases in 16–19 mA/cm^2 range after deposition. This increment of Icc is done at improvement of absorption and the passive affect of hydrogen present during the layer deposition.

Figure 3 presents External Quantum Efficiency of our cells and the one of standard cell (300 µm thick). For wavelength up to 600 nm, absorption of photons is uncompleted. This one explains oneself by the weak thickness of silicon layer.

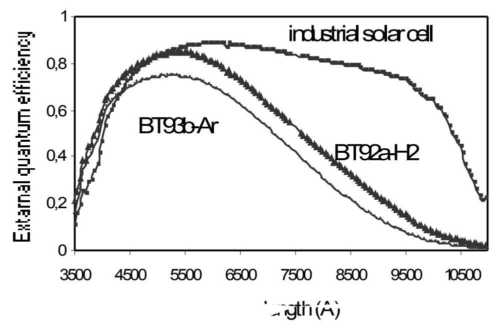


Fig. 3 : External quantum efficiency of solar cells realized from low temperature grown epitaxial layers compared to an industrial solar cell

We observe also that External quantum efficiency is more important in the case of layers obtained under hydrogen flow (BT92a) compared to these one obtained under argon flow (BT93b). This phenomenon explains the important role of de hydrogen as passive in surface and in volume.

IV–Discussion

An efficiency of 4.7 % has been obtained by solar cell of 12 µm thick. It is limited by the weak value of I_{cc} and also by the value of V_{co} about 450 mV only. This efficiency can be improved: by increment of layer thick and also by fabrication of solar cells at HIT structure based on the formation of heterojunction at amorphous silicon to improve the quality of junction [8].

To increase the epitaxial layer thickness, it's necessary to increase the solubility of Si in the melt; this one can to be thanks at thermodynamic study of phase diagram based of silicon. For instance, in the quaternary system Cu–Si–Sn–Al, the copper is alloyed with aluminum to increase the wetting and with tin to decrease the temperature growth. The solubility > 1at % at 700 °C compared

to this one in pure Sn (0.65 at %) (Figure4). Studies show that weak concentration of copper in

the layer < 10^{17} at/cm^3 not damage the quality of junction [9]. Figure 4 shows that liquid phase is placed in zone rich Sn (75 % Sn).

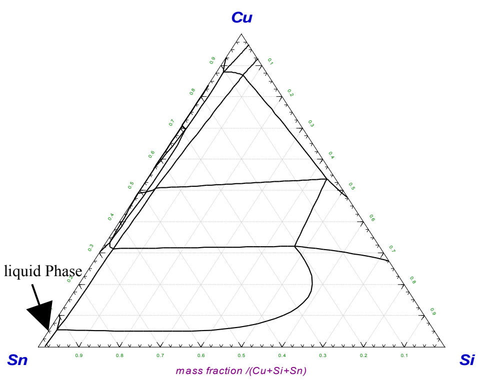


Fig. 4: phase diagram of the ternary system Si-Sn-Cu (with 15%Wt d'Al) at 700°C

HIT technology (Heterojunction with Intrinsic Thin layer) consists to realize amorphous Si deposition doped n+ by PECVD at low temperature (150–200 °C) on single crystalline Si followed by transparent oxide ITO (indium tin oxide) which ensures the function of antireflective coating and the conduction of current of transmitter. Finally, the contacts are ensure by metallization whose the annealing is at 200 °C. This way is promising because it combines the advantages of amorphous and crystalline technologies [8]. It allows ensuring a full technology at low temperature.

V–Conclusion

The growth of smooth and homogeneous layers of 12 at 17 µm of single crystalline Si has been realized by LPE at 800 °C, using two melts system. The photogenerated current (19 mA/cm^2) is limited by the weak thickness of solar cells. So that, to increase the thickness layer, others alloys can be used, like Cu–Si–Sn–Al. Using of HIT structures, it is possible to ensure a low temperature complete technology to realize of solar cells on single crystalline Si thin films.

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7–Acknowledgements

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